LOGIC ANALYSIS SYSTEM FOR LOGIC EMULATION SYSTEMS

Abstract of the Disclosure

A portion of a logic emulation system is configured to sample logic values from the portion of the emulation system that is used to emulate the user digital logic design. These sampled values are then multiplexed by the emulation system to a logic analysis device. Typically, this is a commercially-available logic analyzer. To achieve this functionality, the emulation system is provided with a clock signal that has a higher frequency than the emulation clock signal received from the target or user system. This high speed clock signal is provided to logic analyzer as a strobe signal and controls the transfer of words of logic values from the emulation system to the logic analyzer. As a result, the number of signals that the logic analyzer can effectively sample for a cycle of the emulation clock is increased. Each probe of the logic analyzer can now receive multiple time-division multiplex logic values for each emulation clock cycle thus, increasing the width of logic analysis that can be performed on a particular emulation system with the conventional logic analyzers.